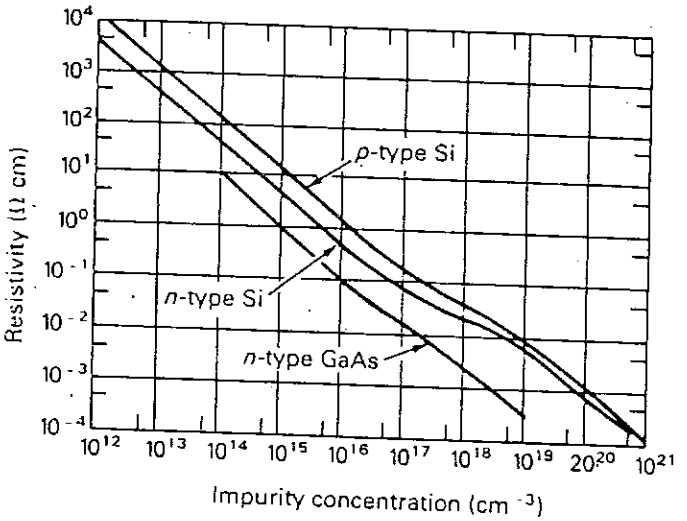
Appendix J

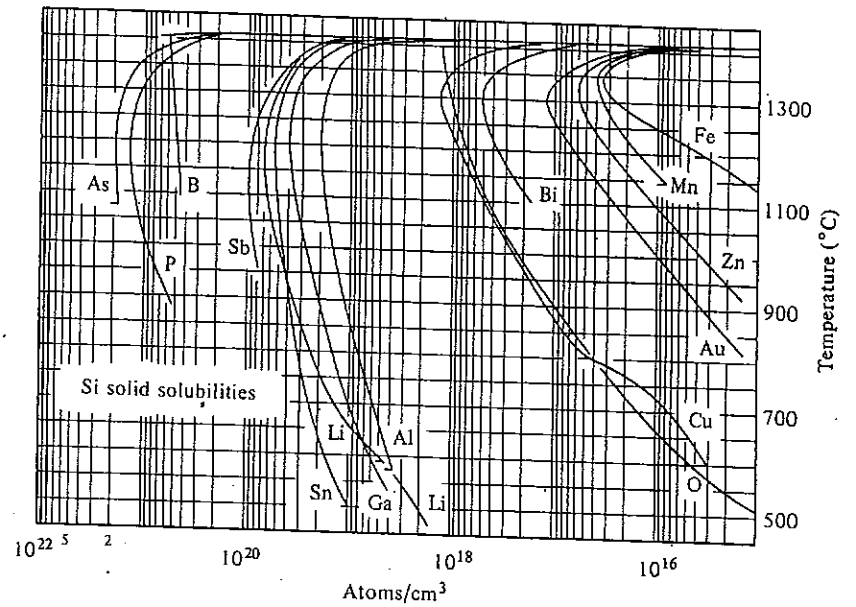
ELECTRICAL RESISTIVITY VERSUS IMPURITY CONCENTRATION AT 300°K FOR SILICON AND GALLIUM ARSENIDE

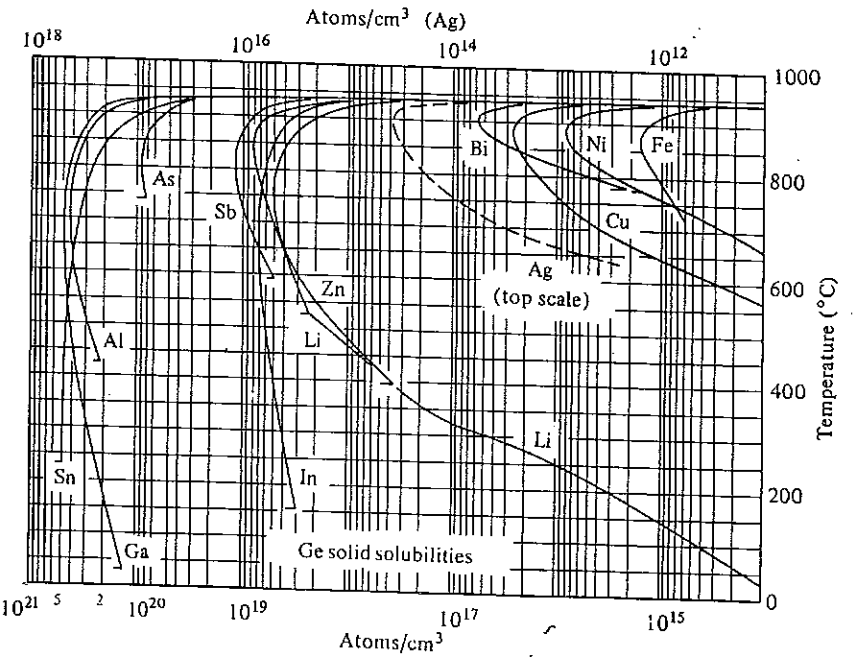
Adapted from S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. (Wiley, New York, 1981), p. 32.



APPENDIX K

SOLID SOLUBILITIES OF IMPURITIES IN "Si" & "Ge"





BAND GAP Vs. LATTICE CONST.

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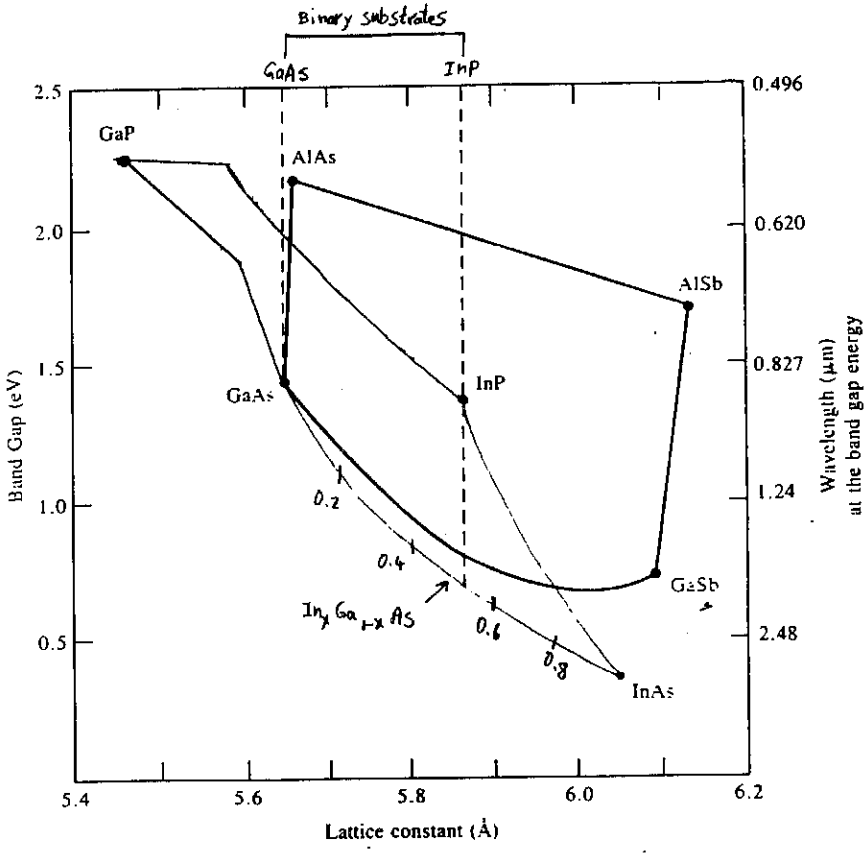
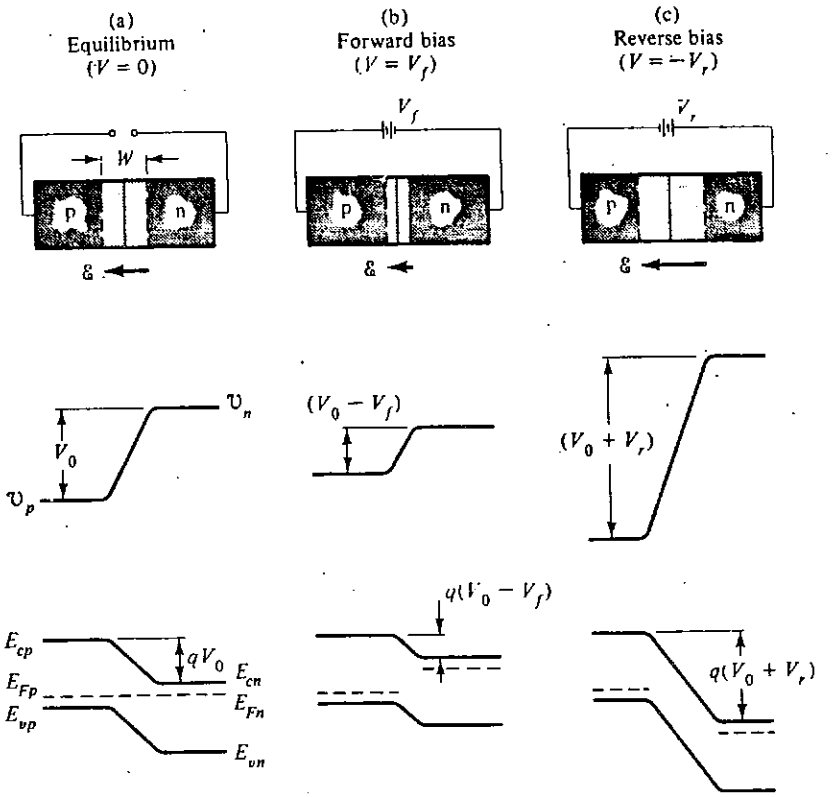


Relationship between band gap and lattice constant for alloys in the InGaAsP and AlGaAsSb systems. The dashed vertical lines show the lattice constants for the commercially available binary substrates GaAs and InP. For the marked example of $In_xGa_{1-x}As$, the ternary composition $x = 0.53$ can be grown lattice-matched on InP, since the lattice constants are the same. For quaternary alloys, the compositions on both the III and V sublattices can be varied to grow lattice-matched epitaxial layers along the dashed vertical lines between curves. For example, $In_xGa_{1-x}As_yP_{1-y}$ can be grown on InP substrates, with resulting band gaps ranging from 0.75 eV to 1.35 eV and with corresponding wavelengths for light emission from 1.65 μm to 0.9 μm.

Appendix M



	Particle flow	Current	Particle flow	Current	Particle flow	Current
(1)	→	→	→	→	→	→
(2)	←	←	←	←	←	←
(3)	←---	---→	←-----	-----→	←-	-→
(4)	---→	←---	---→	←---	---→	←---

(1) Hole diffusion
(2) Hole drift
(3) Electron diffusion
(4) Electron drift

Effects of bias at a p-n junction; transition region width and electric field, electrostatic potential, energy band diagram, and particle flow and current directions within W for (a) equilibrium, (b) forward bias, and (c) reverse bias.

Appendix "P" - Additional Graphs

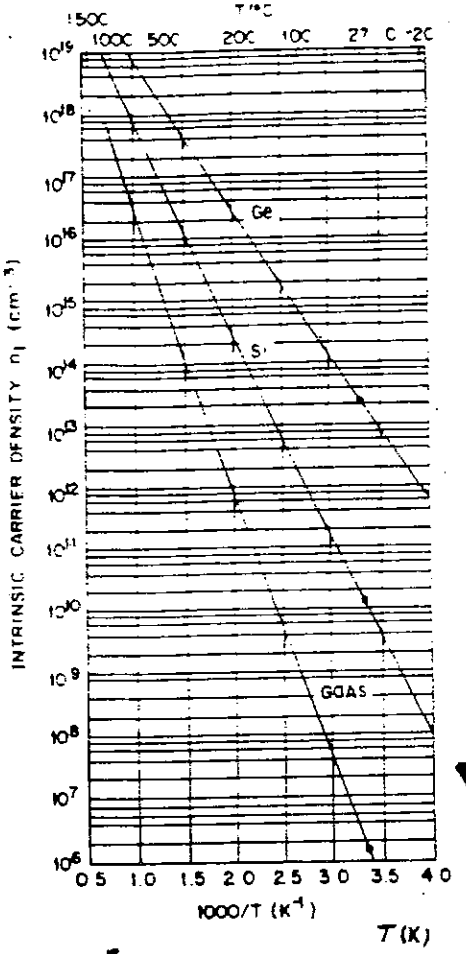
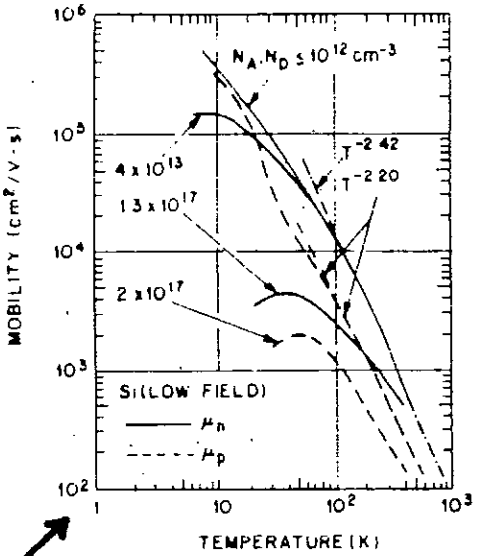


Fig. 11 Intrinsic carrier densities of Ge, Si, and GaAs as a function of reciprocal temperature (After Thurmond, Ref. 20)



Mobility of electrons and holes in Si as a function of temperature.

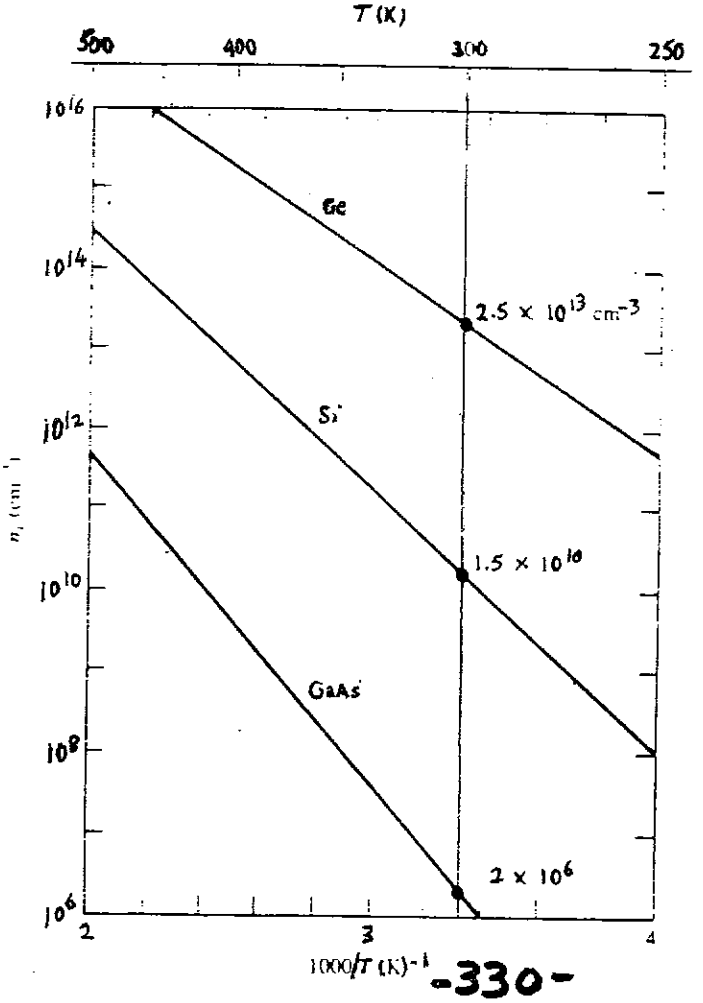


Figure 3-17 Intrinsic carrier concentration for Ge, Si, and GaAs as a function of inverse temperature. The room temperature values are marked for reference.

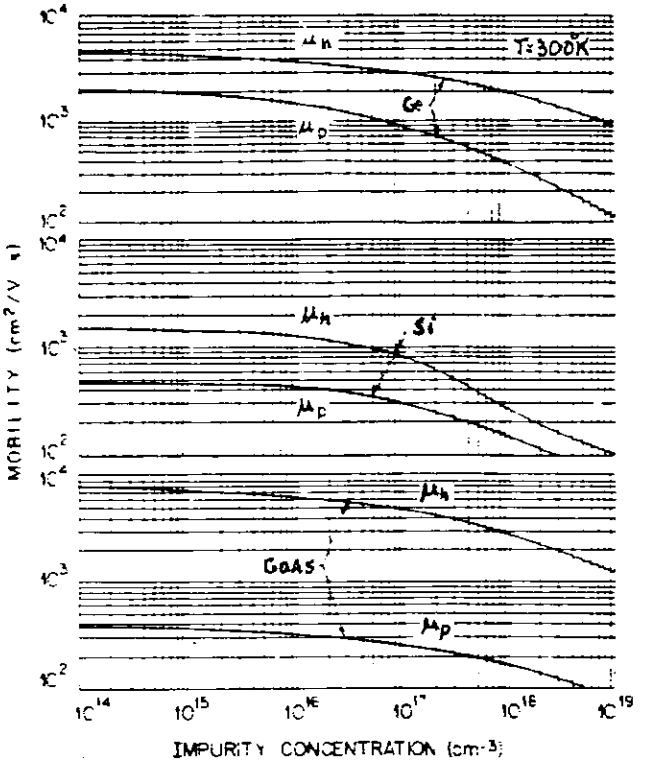
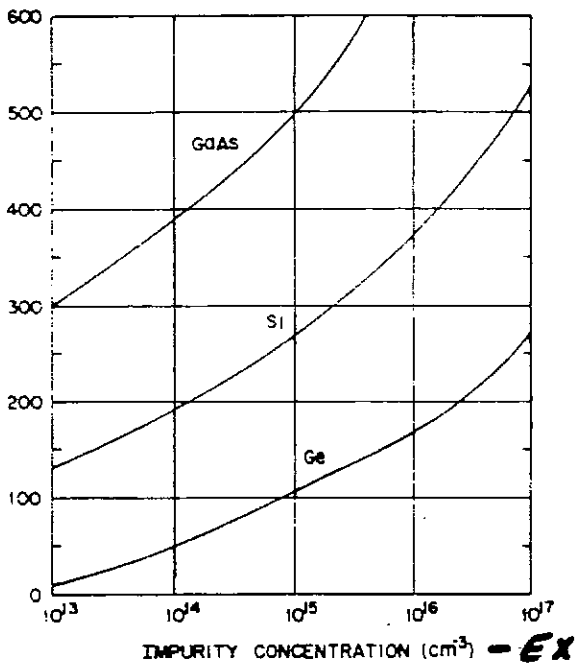


Fig 18 Drift mobility of Ge Si and GaAs at 300 K versus impurity concentration (After Casey and Panish Ref 9 Prince Ref 36 Beadle Plummer and Tsai Ref 36)



$T°(K) = 273 + T(°C)$

Fig. 12 Intrinsic temperature as a function of background concentration.

Extrinsic S/C

T_i = Temp. at which material becomes intrinsic

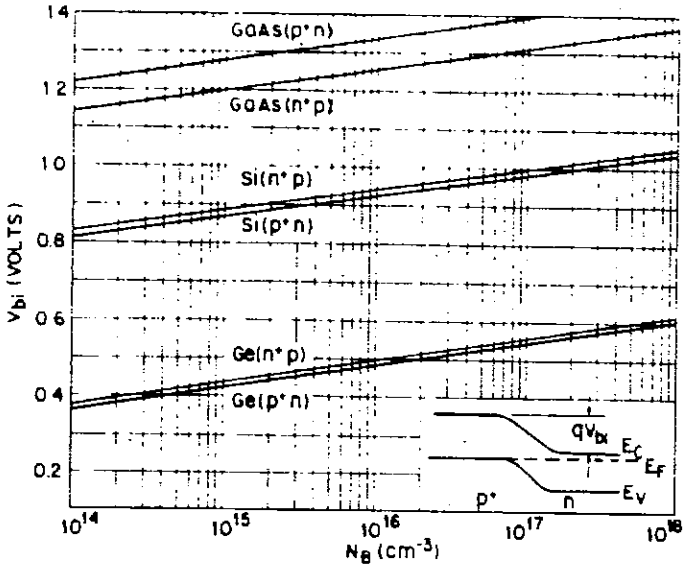


Fig. 11 Built-in potential for one-sided abrupt junctions in Ge, Si, and GaAs where p^+ is for the heavily doped p side and n^+ is for the heavily doped n side. The background doping N_B is for the impurity concentration of the lightly doped side.

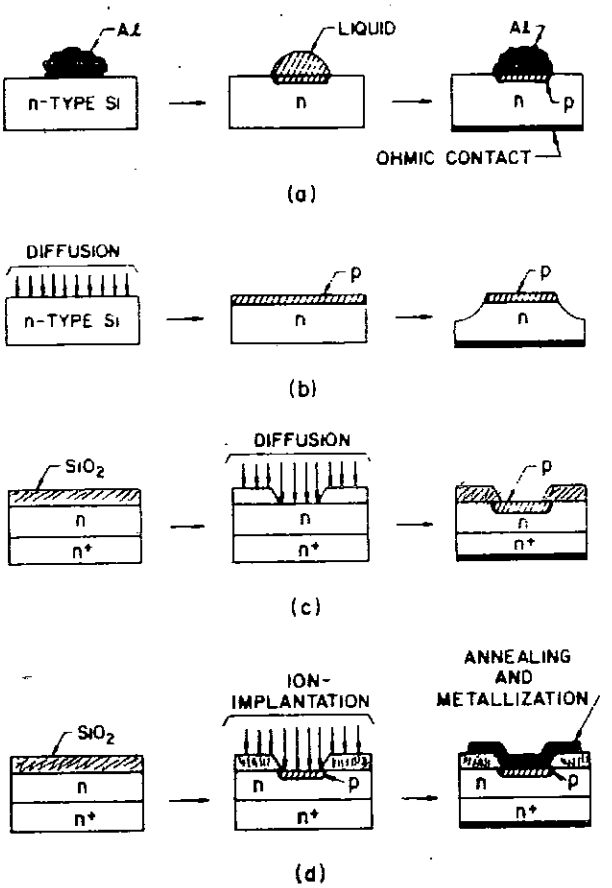


Fig. 1 Some device fabrication methods. (*a*) Alloyed junction. (*b*) Diffused mesa junction. (*c*) Diffused planar junction on epitaxial substrate. (*d*) Ion implantation.